claims:

1. A method of monitoring a reduction in thickness of a bonded semiconductor wafer pair comprised of a first and a second wafer (1, 2), the method comprising
   - forming a test structure (4,5,6,7,8,9), defined by a systematic row of a plurality of trenches having different widths in a defined manner, in an (active) wafer (2), said wafer receiving an active circuit in a later stage;
   - wherein a targeted thickness (h6;h7) of the active wafer (2) during the removal corresponds to a depth (t6;t7) of a reference trench (6;7) of the trenches of the test structure, said reference trench (6) being flanked by shallower and deeper trenches, in particular by a neighbouring shallower and a neighbouring deeper trench (5,7);
   - bonding the active wafer (2) with a side (2a), in which the test structure is formed, onto the second wafer of the semiconductor wafer pair, in particular onto a carrier wafer (1);
   - performing a material removal process, in particular a polishing process, from the backside of the active wafer (2) until the reference trench (6) is exposed, which is optically detectable and is optically detected, respectively for monitoring the reduction in thickness of the first wafer (2).

2. The method of claim 1, wherein the systematic row comprises trenches (4 to 9) of different depths.

3. The method of claim 2, wherein the deep trenches are formed in an etch process using an etch mask having openings of different widths for the trenches of different widths, in particular prior to bonding the active wafer (2) onto the carrier wafer (1).

4. The method of claim 1, wherein the trenches (4 to 9) are not filled, that is, are unfilled or open, prior to bonding the active wafer (2).

5. The method of claim 1, wherein the active wafer (2) is a wafer formed of a semiconductor crystal, in particular formed of silicon.

6. The method of claim 1, wherein the carrier wafer (1) at least comprises an insulating layer, in particular formed of silicon dioxide.

7. The method of claim 1, wherein the systematic row is a sequence of trenches, in particular parallel trenches, that become continuously shallower or continuously deeper.

8. The method of claim 1 or 7, wherein the trenches are formed as stripe-like trenches, and wherein the respective depths increase as the widths increase.

9. The method of claim 1, wherein prior to reaching the bottom (6a) of the reference trench, that is, prior to exposing the bottom of the reference trench (6), the removal process is interrupted at least once for optical monitoring or observation (30).

10. A device for monitoring a reduction in thickness of a bonded semiconductor wafer pair comprised of a first and a second wafer (1,2), comprising
- a test structure (4,5,6,7,8,9) of a systematic row of a plurality of trenches having different widths in a defined manner and formed in the first wafer (2), said first wafer for receiving an active circuit in a later stage, wherein
- a targeted thickness (h7) of the active wafer (2) during the removal corresponds to a depth (t7) of a reference trench (7) of the test structure;
- said active wafer (2) is bonded with a side (2a), in which the test structure is or was formed, onto the second wafer of the semiconductor wafer pair, in particular onto a carrier wafer (1);
- for performing a material removal process, in particular a polishing process, from the backside of the active wafer (2) until the reference trench (7), in particular the bottom (7a) of the reference trench, is exposed; and
- an optical device (30) for monitoring the reduction in thickness.

11. The device of claim 10, wherein the trenches (4 to 9) are not filled with a fill material.

12. The device of claim 10, wherein systematic row of trenches of different depths also comprises a systematic configuration with respect to the widths of the trenches such that the trenches are broader the more deeply they are formed in the first wafer.

13. The device of claim 10 or the method of claim 1, wherein the targeted thickness is the desired or predefined target thickness.

14. The method of claim 9 or 1, wherein the removal process, in particular the polishing process, performed from the backside, is terminated when an optical observation (30) reveals exposure of the reference trench (6), that is exposure is detectable by the optical device from the backside of the active wafer (2).

15. The device of claim 10 or the method of claim 1, wherein the reference trench (6;7) is located in a central region of the systematic row and on one side of the reference trench is located at least one or more trenches of smaller depth and at the other side of the reference trench is located at least one or more trenches of greater depth.

16. The device or method of claim 15, wherein on one side is located at least one or more trenches of smaller width and on the other side is located at least one or more trenches of greater width.

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